

[Serial No.: 09/317,156]

QJ read and a write bit for indicating whether a corresponding memory access slot is one of a read and write slot.

Q3 15. (Amended) The method according to claim 13, wherein the storing step includes storing into the slot-to-port assignment configuration a wrap-around bit that returns the sequence to a first memory access slot at a start of the sequence from an "Nth" memory access slot.

BK 17. (Amended) A switched network system comprising:
a first memory for storing a plurality of programmable system settings;
a second memory for storing data packets;
a network switch having a plurality of ports configured for transferring data packets, the network switch including:
(1) an external memory interface configured for transferring data packets between the network switch and the second memory; and
(2) a scheduler for selectively assigning memory access slots to respective ports based on a selected one of the plurality of programmable system settings stored in the first memory; and
a system controller for supplying the selected one of the plurality of programmable system settings to the network switch.

Q4 18. (Amended) The switched network system according to claim 17, wherein the external memory interface includes a memory access slot assignment table memory.